A NEW ANALYTICAL AND SCALEABLE NOISE MODEL FOR HFET

R. Reuter[+] and F. J. Tegude[*]

[+]Fraunhofer Institute for Applied Physics, 79108-Freiburg, Tullastr. 72, Germany
[*]Gerhard-Mercator-University Duisburg, Solid-States Electronics Department, 47057-Duisburg, Kommandantenstr. 60, Germany

ABSTRACT

In this paper an analytical noise model for HFET, based on the physical interpretation of the bias dependence of the equivalent intrinsic noise sources [1], is presented. This model is bias-dependent and scaleable with the gate-geometry and allows the prediction of all noise parameters using two device dependent parameters in a wide bias range.

INTRODUCTION

An accurate noise model for the prediction of all noise parameters in a wide bias and frequency range is a special task of interest in the actual research areas [2, 3]. In this paper we present a new approach for an analytical noise model. The model is based on an extended temperature noise model which includes effects of gate-leakage current and especially of impact ionization on the noise behaviour of HFET [1, 4]. Using two bias- and gate-geometry independent parameters the behaviour of the main intrinsic noise sources can be described by simple analytical equations. In this paper the values of these two parameters (K_d, K_g) are derived using measured and modeled noise parameters of InAlAs/InGaAs/InP-HFET in a frequency range from 2 GHz up to 18 GHz (atn & HP8970B). It is shown that a set of two independent modeled noise parameters is sufficient for the prediction of the scaleable noise behaviour in a wide bias range. Furthermore, the derived equations form the basis for a new geometry scaling of all noise parameters.

MODEL

In [1] it is presented that the enhanced temperature noise model (fig. 1) gives excellent agreement between measured and modeled noise parameters. Furthermore, it has been shown [1, 5, 6] that the investigation of the equivalent intrinsic noise sources gives an extremely powerful tool for the understanding of the device physics. At bias conditions of interest, the influence of impact ionization and gate-leakage currents on the small-signal and noise performance is negligible, so that so main noise contribution is caused by channel- and output noise sources (normalized to 1 Hz bandwidth):
equivalent intrinsic channel noise voltage:

$$v_{g,n} = \sqrt{4 \cdot k \cdot T_g \cdot R_{gs}}\,, \tag{1}$$

equivalent intrinsic output noise current:

$$i_{d,n} = \sqrt{4 \cdot k \cdot \frac{T_d}{R_{ds}}}\,, \tag{2}$$

with $k = 1.380662 \cdot 10^{-23} \frac{Ws}{K}$ (Boltzmann constant).
If the equivalent output noise current $i_{d,n}$ is plotted in dependence on the shot noise drain current (fig. 2), it can be seen that the bias behaviour can be approximated by a simple analytical expression:

$$\begin{aligned} i_{d,n} &= \sqrt{4 \cdot k \cdot \frac{T_d}{R_{ds}}} \\ &\cong K_d^* \cdot \left(\sqrt{2 \cdot q \cdot |I_D|} - \sqrt{2 \cdot q \cdot I_{D,d}}\right), \quad I_{D,d} \geq 0 \end{aligned} \tag{3}$$

with I_D the drain-current.
To obtain a comparable relation for the equivalent channel noise voltage $v_{g,n}$, it is necessary to transform this noise contribution to a noise measure of the output circuit of the HFET.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

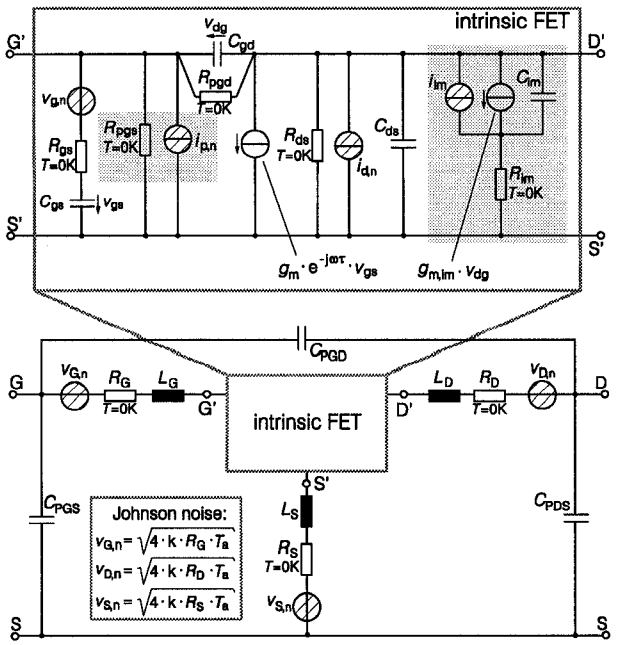

Fig. 1: Intrinsic and extrinsic small-signal- and noise equivalent circuit of HFET including modeling of gate-leakage current and impact ionization on the RF- and noise behaviour.

This can be done by multiplying $v_{g,n}$ with the ratio of the square of the transconductance gm and the intrinsic current gain cut-off frequency f_T. Now, the mathematical interpretation of the bias behaviour of the transformed channel noise voltage $v_{gt,n}$ (fig. 3) is given by:

$$v_{gt,n} = \sqrt{4 \cdot k \cdot T_g \cdot R_{gs}} \cdot \frac{g_m^2}{f_T} \cong K_g^* \cdot \left(\sqrt{2 \cdot q \cdot |I_D|} - \sqrt{2 \cdot q \cdot I_{D,g}} \right), \quad I_{D,g} \geq 0 \tag{4}$$

Using the small-signal equivalent elements and the device parameter, K_g^*, $I_{D,g}$, K_d^* and $I_{D,d}$ the noise behaviour (all noise parameters) can be predicted in a wide bias range. The parameters K_g^* and K_d^* are bias independent but gate-geometry dependent. To investigate the geometry dependence (gate-length L_g and gate-width W_g) of these parameters, the equivalent intrinsic noise sources of transistors with varying gate-width and gate-length have been extracted and analyzed in dependence on the shot noise drain current (fig. 4).

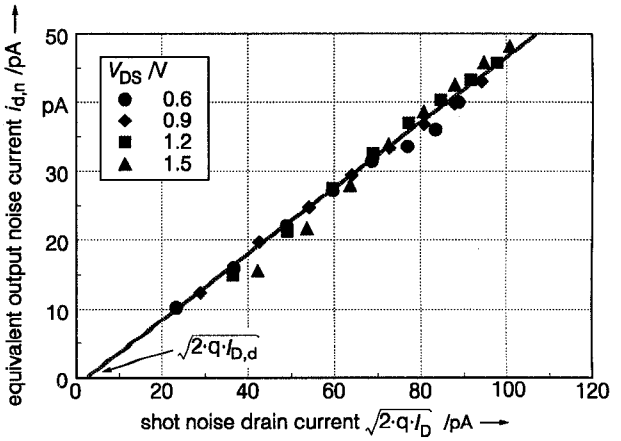

Fig. 2: Equivalent output noise current $i_{d,n}$ in dependence on the shot noise drain-current for a typical InP-based HFET ($L_g = 0.5$ µm, $W_g = 80$ µm). Points indicate measured/extracted values, line represents simple linear approximation.

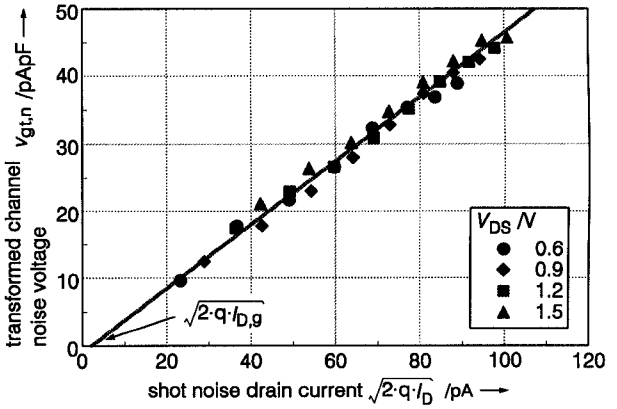

Fig. 3: Transformed equivalent channel noise voltage $v_{gt,n}$ in dependence on the shot noise drain current for a typical InP-based HFET ($L_g = 0.5$ µm, $W_g = 80$ µm). Points indicate measured/extracted values, line represents simple linear approximation.

Based on these investigations following final analytical expressions can be derived for the equivalent intrinsic noise sources:

$$i_{d,n} = \sqrt{4 \cdot k \cdot \frac{T_d}{R_{ds}}} \cong K_d \cdot \left(\sqrt{2 \cdot q \cdot |I_D|} - \sqrt{2 \cdot q \cdot I_{D,d}} \right), \tag{5}$$

$$v_{g,n} = \sqrt{4 \cdot k \cdot T_g \cdot R_{gs}} \cong \frac{K_g \cdot W_g \cdot L_g \cdot f_T}{g_m^2} \left[\sqrt{2 \cdot q \cdot |I_D|} - \sqrt{2 \cdot q \cdot I_{D,g}} \right] \quad (6)$$

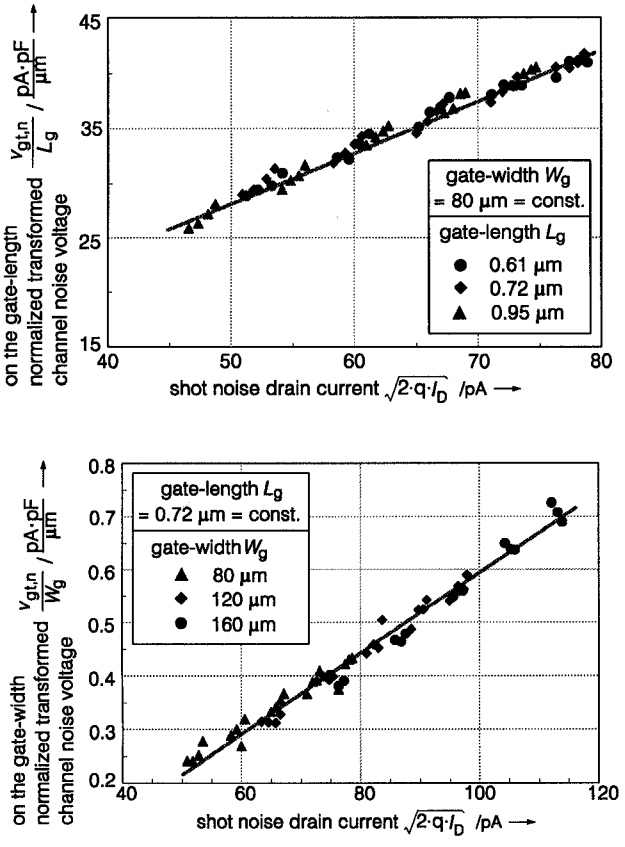

Fig. 4: Normalized transformed equivalent channel noise voltage $v_{gt,n}$ in dependence on the shot noise drain current with a): normalized on the gate-length b): normalized on the gate-width; (T = 300 K, V_{DS} = 0.9 V up to 1.8 V, V_{GS} = -0.3 V up to 0.1 V)

For practical operation the small influence of the parameter $I_{D,d}$ and $I_{D,g}$ can be neglected, so that following equations are sufficient for the prediction of the noise behaviour:

$$i_{d,n} = \sqrt{4 \cdot k \cdot \frac{T_d}{R_{ds}}} \cong K_d \cdot \sqrt{2 \cdot q \cdot |I_D|}, \quad (7)$$

$$v_{g,n} = \sqrt{4 \cdot k \cdot T_g \cdot R_{gs}} \cong K_g \cdot W_g \cdot L_g \cdot \sqrt{2 \cdot q \cdot |I_D|} \cdot \frac{f_T}{g_m^2} \cdot \quad (8)$$

GEOMETRY SCALING OF THE NOISE PARAMETERS

To verify the new analytical noise model and to obtain a new scaling method [7] for all noise parameters, which can be easy implemented in any circuit design tool, a simplified intrinsic temperature noise model [8] is used to derive analytical expressions for all noise parameters:

$$F_{min} = 1 + \frac{2}{T_0} \cdot \frac{f}{f_T} \cdot \sqrt{R_{gs} \cdot T_g \cdot \frac{T_d}{R_{ds}}}, \quad (9)$$

$$R_{Q,opt} = \frac{f_T}{f} \cdot \sqrt{R_{gs} \cdot T_g \cdot \frac{R_{ds}}{T_d}}, \quad (10)$$

$$X_{Q,opt} = \frac{1}{f} \cdot \frac{1}{2 \cdot \pi \cdot C_{gs}}, \quad (11)$$

$$R_n = \frac{1}{T_0} \cdot \left(R_{gs} \cdot T_g + \frac{T_d}{R_{ds}} \cdot \frac{1}{g_m^2} \right). \quad (12)$$

These estimations are sufficient for the geometry scaling of the intrinsic noise parameters of HFETs. Using these formulas and the equations (7), (8) a coherence between the intrinsic noise parameters and additional transistor parameters can be derived:

$$F_{min} - 1 = \frac{f}{T_0} \cdot \frac{K_g \cdot K_d}{2 \cdot k} \cdot W_g \cdot L_g \cdot \frac{2 \cdot q \cdot |I_D|}{g_m^2}, \quad (13)$$

$$R_{Q,opt} = \frac{f_T}{f} \cdot \frac{K_g}{K_d} \cdot W_g \cdot L_g \cdot \frac{f_T}{g_m^2}, \quad (14)$$

$$X_{Q,opt} = \frac{1}{f} \cdot \frac{1}{2 \cdot \pi \cdot C_{gs}}, \quad (15)$$

$$R_n = \frac{1}{T_0} \cdot \frac{2 \cdot q \cdot |I_D|}{4 \cdot k \cdot g_m^2} \left[\left(K_g \cdot W_g \cdot L_g \cdot \frac{f_T}{g_m^2} \right)^2 + K_d^2 \right], \quad (16)$$

with q the electron charge = $1.6022 \cdot 10^{-19}$ As and T_0 the reference temperature = 290 K.

With the estimations for the gate-length- and gate-width-scaling of the drain-current I_D, transconductance g_m and gate-source-capacitance C_{gs} listed in Tab. 1, the geometry dependence of the intrinsic noise parameters, shown in Tab. 2, can be obtained.

gate-length dependence	gate-width dependence
$g_m \neq f(L_g) = \text{const.}$	$g_m \propto W_g$
$C_{gs} \propto L_g$	$C_{gs} \propto W_g$
$f_T \propto 1/L_g$	$f_T \neq f(W_g) = \text{const.}$
$I_D \neq f(L_g) = \text{const.}$	$I_D \propto W_g$

Tab. 1: Scaling properties of some small-signal equivalent elements and device parameters.

gate-length dependence	gate-width dependence
$F_{min}\text{-}1 \propto L_g$	$F_{min}\text{-}1 \neq f(W_g) = \text{const.}$
$R_{Q,opt} \propto 1/L_g$	$R_{Q,opt} \propto 1/W_g$
$X_{Q,opt} \propto 1/L_g$	$X_{Q,opt} \propto 1/W_g$
$R_n \neq f(L_g) = \text{const.}$	$R_n \propto 1/W_g$

Tab. 2: Derived scaling behaviour of the intrinsic noise parameters.

The validity of the presented method is clearly demonstrated by the comparison of measured extrinsic noise parameters of InP based HFET with varying gate-geometry.

CONCLUSION

A new analytical scaleable noise model for HFET is presented. The novel approach is based on an extended temperature noise model and the analysis of the bias dependence of the equivalent intrinsic noise sources. Intensive comparison with measured noise parameters of InAlAs/InGaAs/InP-HFET demonstrates the capability of the presented method. Furthermore, a simple practical estimation for the geometry scaling of all noise parameters can be obtained using the new model. Finally, the model is easy to implement in any large signal model which allows an access to the noise and RF-behaviour simultaneously.

AKNOWLEDGEMENT

The work was performed at the Gerhard Mercator University Duisburg, 47057 Duisburg, Germany and was supported by the Sonderforschungsbereich 254.

REFERENCES

[1] R. Reuter, M. Agethen, U. Auer, S. van Waasen, D. Peters, W. Brockerhoff, F. J. Tegude; Investigation and Modeling of Impact Ionization with Regard to the RF- and Noise Behaviour of HFET. IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 6, p. 977-983, 1997

[2] B.-U. H. Klepser, C. Bergamaschi, M. Schefer, C. G. Diskus, W. Patrick, W. Bächthold; Analytical Bias Dependent Noise Model for InP HEMT's. IEEE Transactions on Electron Devices, vol. 42, no. 11, p. 1882-1889, 1995

[3] Y. Ando, A. Cappy, K. Maruhashi, K. Onda, H. Miyamoto, M. Kuzuhara; Noise Parameter Modeling for InP-Based Pseudomorphic HEMT's. IEEE Transactions on Electron Devices, vol. 44, no. 9, p. 1367-1374, 1997

[4] R. Reuter, S. van Waasen, F. J. Tegude; A new Noise Model of HFET with Special Emphasis on Gate-Leakage. IEEE Electron Device Letters, vol. 16, no. 2, p. 74-76, 1995

[5] R. Reuter, S. van Waasen, D. Peters, U. Auer, W. Brockerhoff, F. J. Tegude; A new temperature noise model of HFET with special emphasis on a gate-leakage current and investigation of the bias dependence of the equivalent noise sources; Conference Proceedings of the 25th European Microwave Conference, Bologna, Italy, p. 205-210, 1995

[6] L. Klapproth, A. Schader, G. Boeck; A Bias Dependent HEMT Noise Model. Conference Proceedings of the MTT-S, Denver, USA, p. 881-884, 1997

[7] A. Gasmi, B. Huyart, E. Bergeault, L. P. Jallet; A New Calculation Approach of Transistor Noise Parameters as a Function of Gatewidth and Bias Current. IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 3, p. 338-344, 1997

[8] W. Pospieszalski; Modelling of Noise Parameters of MESFET's and MODFET's and Their Frequency and Temperature Dependence. IEEE Transactions on Microwave Theory and Techniques, vol. 37, no. 9, p. 1340-1350, 1989